A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM

Daeyong Shim, Hyunsik Jeong, Hyunjoong Lee, *Member, IEEE*, Cyuyeol Rhee, Deog-Kyoon Jeong, *Senior Member, IEEE*, and Suhwan Kim, *Senior Member, IEEE*

***Abstract*—Smaller transistors mean that capacitors are charged less uniformly, which increases the self-refresh current in the DRAMs used in mobile devices. Adaptive self-refresh using an on-chip thermometer can solve this problem. We propose an on-chip CMOS thermometer specifically designed for controlling the refresh period of a DRAM. This thermometer includes a novel temperature sensor which has been implemented and integrated into an LPDDR2 chip. The LPDDR2 chip is fabricated in a 44-nm DRAM process. The sensor has a temperature sensitivity of -3.2 mV/°C, over a range of 0 °C to 110 °C. Its resolution is 1.94 °C and is only limited by the 6.2-mV step of the associated resistor ladder not by its own design. The linearity of the sensor permits one-point calibration, after which the errors in 61 sample circuits ranged between -1.42 °C and $+2.66$ °C. The sensor has an active area of 0.001725 mm^2 and consumes less than 0.36 μW on average with a supply of 1.1 V. At its lowest operating temperature, this thermometer reduces the IDD6 current of the LPDDR2 chip by almost half.**

***Index Terms*—Low-power, mobile DRAM, self-refresh, temperature sensor, thermometer.**

I. Introduction

HIGH-END smartphones and large-screen tablet PCs with dual-core or quad-core CPUs are leading rapid growth in the use of DRAM in mobile devices. This DRAM needs to be fast, and also energy efficient, to prolong battery life even. Mobile double data-rate (DDR) DRAM, known as LPDDR2, is being rapidly adopted in mobile devices, as it consumes less power in standby mode than the DDR DRAM used in many PCs.

However, the required DRAM density in devices such as 2 GB in high-end smartphones makes it difficult to keep power consumption low, because the self-refresh current of the DRAM, during both standby and operation, rises with both capacity and density. The operating current, required to sense and restore data, is inversely proportional to the internal refresh period, which is determined by the data retention capability of a DRAM cell. The period for which a cell retains data decreases as the temperature rises, and the maximum self-refresh period is theoretically limited by the retention capability at the highest operating temperature. In practice, an on-chip thermometer can be used to measure the temperature, and then the operating current in the self-refresh period is reduced by selecting the appropriate internal refresh period [1], [2]. This type of temperature-based control of the self-refresh period is called auto temperature-compensated self-refresh (TCSR).

Most temperature sensors can be put into one of two categories [3]: conventional sensors, which are based on proportional-to-absolute temperature (PTAT) or complementary-to-absolute temperature (CTAT) principles and employ a bipolar junction transistor (BJT) [2] or a CMOS transistor [1]; and "alternative" sensors, which measure temperature-dependent time delay of a logic gate [4]. Examples of conventional designs are high-resolution thermometers implemented using a PTAT current generator and an analog-to-digital converter (ADC) [5], [6]. After calibration, they can typically achieve better than ± 1°C accuracy, and an enhanced accuracy of ± 0.1 °C has reportedly been achieved by applying dynamic element matching and offset cancellation [7]. Even though a conventional temperature sensor of these thermometers is simple and precise, it requires a high-resolution ADC to achieve an accurate digital output, bringing the penalties of increased power consumption, circuit complexity, and chip area. Alternative designs use inverter delay cells and a time-to-digital converter (TDC) to measure the time that it takes for the current to charge a capacitor to a fixed threshold voltage [4], [8], [9], [10]. After an initial batch calibration, low-cost one-point calibration of individual circuits of this type is sufficient to achieve accuracies of a few degrees over a range from 40 °C to 90 °C [8]. Using two-point calibration improves the accuracy to about ± 1 °C, between -10 °C and 30 °C [9]. One of the alternative designs measures the temperature-dependent propagation delay of a chain of inverters [4]. This type of sensor achieves an accuracy of -0.7 to $+0.9$°C after two point calibration. An all-digital CMOS temperature sensor based on a dual-DLL has also been used to monitor the thermal profile of a microprocessor, as well as to control the self-refresh of a DRAM [3]. A thermometer for use in self-refresh control of DRAM does not have to be able to measure every temperature in the operating range accurately [11], [12]. Although more efficient than conventional thermometers, TDC-based thermometers still occupy

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D. Shim was with the Department of Electrical Engineering, Seoul National University, Seoul 151-744, Korea. He is now with SK Hynix, Icheon, 467-701, Korea.

H. Jeong is with SK Hynix, Icheon, 467-701, Korea.

H. Lee, C. Rhee, D.-K. Jeong, and S. Kim are with the Department of Electrical Engineering, Seoul National University, Seoul 151-744, Korea (e-mail: suhwan@snu.ac.kr).

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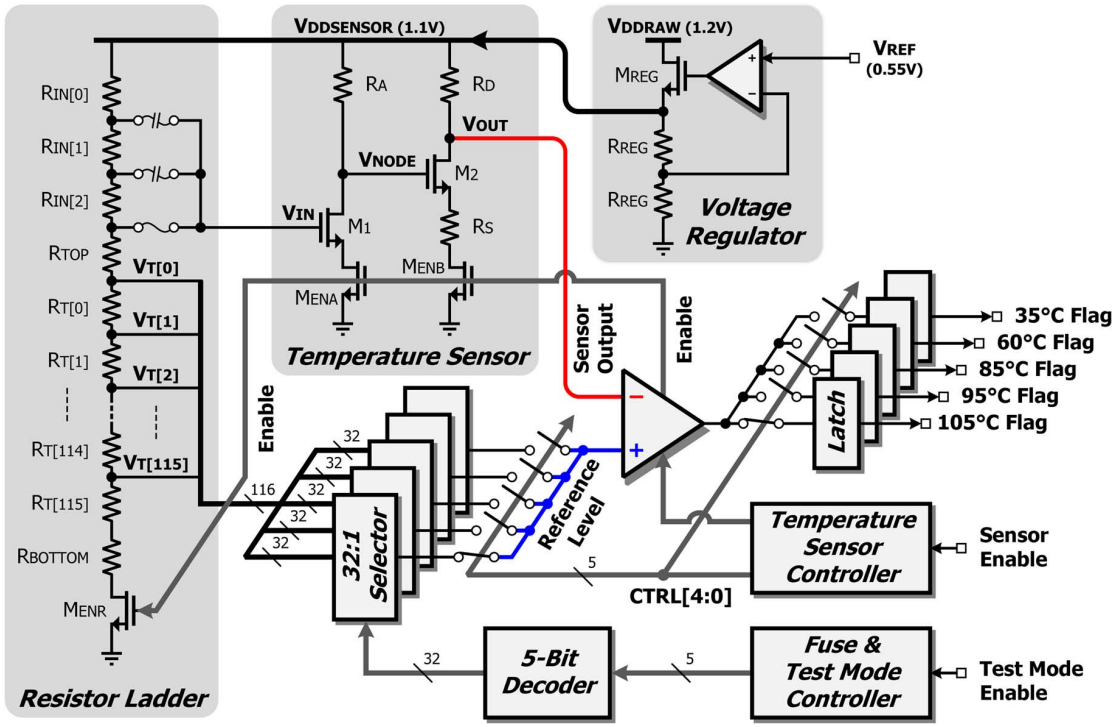

Fig. 1. Proposed on-chip CMOS thermometer.

a considerable area and require a relatively large amount of power, and their susceptibility to process variations inevitably requires a costly calibration process [4]. It is sufficient to detect the specific temperature with respect to a fixed set of reference temperatures, provided that this information should be acquired quickly by a circuit with a low power and small area consumption. In addition, a low-cost one-point calibration is desirable, even at some cost in accuracy.

We propose a thermometer including a novel temperature sensor which generates a CTAT voltage either without using BJT or conventional CMOS. It achieves a good accuracy and is relatively insensitive to process variation because it only contains NMOS transistors and n+ active resistors. Since the temperature dependency of temperature-dependent characteristics of these transistors and resistors are known, the characteristics of the sensor output can easily be predicted and compensated against process variations by selecting appropriate resistor values and threshold voltages for the NMOS transistors. This feature permits one-point calibration, favoring commercial application, and the application of this design to LPDDR2 memory products has been demonstrated.

The remainder of this paper is organized as follows. The design and operation of the proposed thermometer are introduced in Section II. In Section III, we analyze the operational principles of its temperature sensor circuit in detail, and, in Section IV, we present the simulation and experimental results for the temperature sensor and thermometer which contains it. Finally, we conclude the paper in Section V.

II. Overall Architecture of the Thermometer

As shown in Fig. 1, the thermometer is composed of a temperature sensor, a resistor ladder, five 32:1 selectors, a voltage regulator, a comparator, five latches, a temperature sensor controller, and a controller for fuse and test modes.

The voltage regulator receives a temperature-independent reference voltage V_{REF} of 0.55 V from the main DRAM system and maintains the internal supply voltage V_{DDSENSOR} at 1.1 V; this stabilized voltage isolates every block of the thermometer from the supply noise. The temperature sensor generates the voltage V_{OUT} which linearly tracks the temperature. The detailed operational principle of the sensor will be described in Section III. To process the output of the sensor, the resistor ladder generates five reference voltages which correspond to the five temperatures 105 °C, 95 °C, 85 °C, 60 °C, and 35 °C. The temperature sensor controller sequentially selects each of these reference voltages for comparison with the sensor output. The results of these comparisons are latched to set one of five temperature flags. These flags are routed to the DRAM controller to set the appropriate refresh period.

To compensate for process variations, one of the voltage levels from the resistor ladder is selected as the input V_{IN} of the temperature sensor by trimming a fusible links, and the other voltages $V_{\mathrm{T}}[115:0]$ provide five reference levels. Each of these reference voltages is adjustable over 32 increments with a step of 6.2 mV. When test mode is enabled, each of the five levels is trimmed as close as possible to its design value by the fuse and test mode controller and the 32:1 selectors. To extend trimming range, the inputs to five 32:1 selectors are partially overlapped with one another. After trimming is complete, the selected levels are permanently set by fusible links. Once set, these fixed levels are unaffected by temperature changes because they are derived from the temperature-independent internal supply voltage V_{DDSENSOR}. To minimize power consumption, the temperature sensor controller uses the *Enable* signal to start and stop the temperature sensor, the resistor ladder, and the

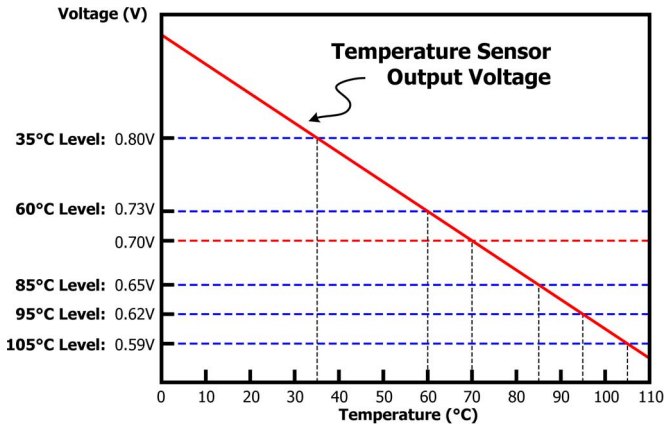

Fig. 2. Expected sensor output voltage with reference levels against temperature.

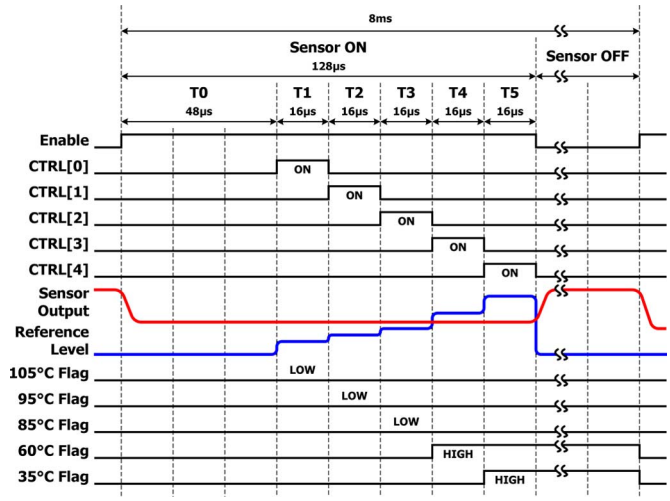

Fig. 3. Timing diagram of the input and output signals of the thermometer at a temperature of 70 °C.

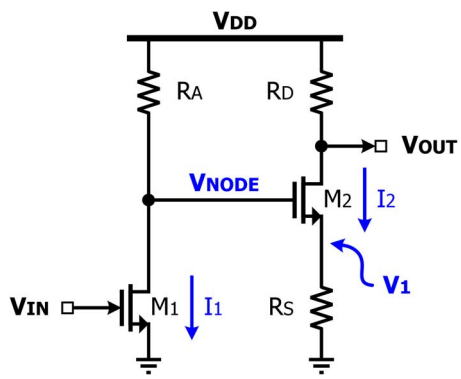

Fig. 4. Temperature sensor circuit.

comparator, so that they only operate during 128 μs of the 8 ms update cycle at the self-refresh mode of the mobile DRAM.

Figs. 2 and 3 illustrate how this circuit responds to a temperature of 70 °C. Fig. 2 shows the sensor output voltage and the five reference levels with respect to the temperature variation. Since each reference level of the five reference temperatures is set equal to the output voltage of the temperature sensor at the corresponding temperature, it is evident from the figure that the output voltage at 70 °C lies between the reference level at 85 °C and the reference level at 60 °C. Fig. 3 depicts the timing diagram of all of the major input and output signals of the thermometer, which is operating at the given temperature. A temperature measurement begins when the *Enable* signal goes high. During an initial period $T0$, which lasts for 48 μs, all of the analog blocks, including the temperature sensor, are powered on and the sensor output voltage settles. Since the temperature does not change abruptly, the variation of the settled output voltage is negligible within the whole sensing time of one cycle, 128 μs. During the five periods from $T1$ to $T5$, each of which lasts for 16 μs, the output voltage is compared with a reference voltage selected from the five possible levels by the switch control signals $CTRL[4:0]$. If the output voltage is lower than the selected reference level throughout each period, the comparator output goes high and is latched to set the appropriate flag for that reference temperature. In the example shown in Fig. 3, the flags for 105 °C, 95 °C, and 85 °C stay low during the periods $T1$, $T2$, and $T3$, but these for 60 °C and 35 °C are set and go high during $T4$ and $T5$, because the temperature is 70 °C.

III. Operational Principles of the Temperature Sensor Circuit

Our thermometer uses a novel CTAT voltage generator as the temperature sensor and simple comparators as detectors, so as to reduce power consumption and area. Considering the requirements of the low power consumption and the low supply voltage of below 1.2 V for cost-sensitive LPDDR2 products, the BJT may not be suitable [13], [14]. We use only NMOS transistors and n+ active resistors to improve the temperature sensitivity of the sensor, and reduce its sensitivity to process variation.

Fig. 4 shows a schematic diagram of the temperature sensor, in which the footer transistors that turn the sensor on and off are omitted for simplicity. The NMOS transistor M_1 operates in its triode region, and the NMOS transistor M_2 operates in its saturation region. $R_{\rm A}$, $R_{\rm S}$, and $R_{\rm D}$ are n+ active resistors. $V_{\rm DD}$ is the temperature-independent internal supply voltage of 1.1 V from the voltage regulator. $V_{\rm IN}$ is the input bias voltage, which is selected by the resistor ladder to allow M_1 to operate in its triode region at all process corners and temperatures between 0 °C and 110 °C. This biasing makes the output $V_{\rm NODE}$ of the sensor's first branch increase linearly with temperature. The second branch, which is composed of $R_{\rm D}$, $R_{\rm S}$, and M_2, forms a linear common source amplifier with source degeneration, which amplifies $V_{\rm NODE}$ to $V_{\rm OUT}$ to increase the temperature sensitivity.

Since the threshold voltage $V_{\rm TH}$ and the mobility $\mu_{\rm N}$ of the NMOS transistor are affected by the process and temperature variation, we need to obtain an expression for the output voltage which contains all of these parameters, so as to take account of their effects on the output voltage. First, we derive an equation for $V_{\rm NODE}$ at the output of the first branch. Since M_1 operates in its triode region, the drain current I_1 of M_1 is

$$I_1 = \mu_{N1} C_{\rm OX} \left(\frac{W}{L}\right)_1 \left[(V_{\rm IN} - V_{\rm TH1})\, V_{\rm NODE} - \frac{V_{\rm NODE}^2}{2}\right] \quad (1)$$

where $\mu_{\rm N1}$ is the mobility of M_1, $(W/L)_1$ is its aspect ratio, and $V_{\rm TH1}$ is its threshold voltage. $V_{\rm NODE}$ is written as

$$V_{\rm NODE} = V_{DD} - I_1 R_A. \tag{2}$$

Substituting (1) into (2), we get a closed-form expression for $V_{\rm NODE}$

$$V_{\rm NODE} = V_{\rm IN} - V_{\rm TH1} + \frac{1}{\beta_1 R_A} - \sqrt{\left(V_{\rm IN} - V_{\rm TH1} + \frac{1}{\beta_1 R_A}\right)^2 - \frac{2V_{\rm DD}}{\beta_1 R_A}} \tag{3}$$

where $\beta_1 = \mu_{\rm N1} C_{\rm OX}(W/L)_1$.

Now, we will formulate expressions for the mobility $\mu_{\rm N}$, the threshold voltage $V_{\rm TH}$, and the resistance R in terms of temperature [15] as

$$\mu_N(T) = \mu_{N0}\left(\frac{T}{T_0}\right)^{-m} \tag{4}$$

$$\beta(T) = \beta_0\left(\frac{T}{T_0}\right)^{-m} \tag{5}$$

$$V_{\rm TH}(T) = V_{\rm TH0} - \alpha_{\rm VTH}(T - T_0) \tag{6}$$

$$R(T) = R_0\left[1 + \alpha_R(T - T_0)\right] \tag{7}$$

where T_0 is the reference temperature and T is the temperature. The exponent m in (4) is a constant which can be expressed to have a value from 1.2 to 2; the latter value is frequently used for n-channel devices. From these relationships, β can also be expressed as a function of T, where $\beta_0 = \mu_{\rm N0} C_{\rm OX}(W/L)$. $\alpha_{\rm VTH}$ is a constant which can be expected to have values between 1 and 4 mV/°C, and a commonly used value is 2 mV/°C [15]. $\alpha_{\rm R}$ is a constant which depends on the type of the resistor.

Substituting (4)–(7) into (3), we can express $V_{\rm NODE}$ as the first term of a Taylor expansion given by (8), shown at the bottom of the page. From this equation, we see that $V_{\rm NODE}$ is proportional to temperature, as long as M_1 is operating in its triode region. In this linearized expression, the slope M of the $V_{\rm NODE}$ against temperature mainly depends on $\alpha_{\rm VTH1}$, which is not greatly affected by process variation. We can see that the offset N also depends mainly on $V_{\rm IN} - V_{\rm TH10}$, and $V_{\rm IN}$ can easily be adjusted using the resistor ladder shown in Fig. 1.

Next, we derive the equation of $V_{\rm OUT}$ at the output of the second branch. Since M_2 operates in its saturation region, the drain current I_2 of M_2 is expressed as

$$I_2 = \frac{1}{2}\mu_{N2} C_{\rm OX}\left(\frac{W}{L}\right)_2 (V_{\rm NODE} - V_1 - V_{\rm TH2})^2 \tag{9}$$

where $V_1 = I_2 R_{\rm S}$. $V_{\rm OUT}$ can be written as

$$V_{\rm OUT} = V_{\rm DD} - I_2 R_D. \tag{10}$$

By substituting this equation into (10), we get a closed-form expression for $V_{\rm OUT}$ as

$$V_{\rm OUT} = V_{\rm DD} - \frac{R_D}{R_S}\left[V_{\rm NODE} - V_{\rm TH2} + \frac{1}{\beta_2 R_S}\left\{1 - \sqrt{1 + 2\beta_2 R_S(V_{\rm NODE} - V_{\rm TH2})}\right\}\right] \tag{11}$$

where $\beta_2 = \mu_{\rm N2} C_{\rm OX}(W/L)_2$. Substituting (4)–(7) into (11), we can express $V_{\rm OUT}$ as the first term of a Taylor expansion given by (12), shown at the bottom of the following page. In this linearized expression, the coefficient P of the $V_{\rm OUT}$ against temperature mainly depends on $\alpha_{\rm VTH2}$, which is not greatly affected by process variation. Q mainly depends on $-V_{\rm TH20}$. The effect of nonlinearities on these coefficients, including the temperature dependency of mobility, is mitigated by the large value of $R_{\rm S0}$. By substituting (8) into (12), we finally obtain a linearized expression for $V_{\rm OUT}$ as

$$\begin{aligned} V_{\rm OUT}(T) &\simeq V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[M(T - T_0) + N + P(T - T_0) + Q\right] \\ &= V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[(M + P)(T - T_0) + N + Q\right] \\ &= V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[(\alpha_{\rm VTH1} + \alpha_{\rm VTH2} + e_{Slope})(T - T_0) + \{V_{\rm IN} - (V_{\rm TH10} + V_{\rm TH20}) + e_{\rm Offset}\}\right]. \end{aligned} \tag{13}$$

$$\begin{aligned} V_{\rm NODE}(T) &\simeq M(T - T_0) + N \\ M &= \alpha_{\rm VTH1} + \frac{1}{\beta_{10} R_{A0} T_0}\left[m - \alpha_R T_0 + \frac{(m - \alpha_R T_0)V_{\rm DD}}{\sqrt{\left(V_{\rm IN} - V_{\rm TH10} + \frac{1}{\beta_{10} R_{A0}}\right)^2 - \frac{2V_{\rm DD}}{\beta_{10} R_{A0}}}} - \frac{(1 + \beta_{10} R_{A0} V_{\rm IN} - \beta_{10} R_{A0} V_{\rm TH10})(m - \alpha_R T_0 + \alpha_{\rm VTH1}\beta_{10} R_{A0} T_0)}{\beta_{10} R_{A0}\sqrt{\left(V_{\rm IN} - V_{\rm TH10} + \frac{1}{\beta_{10} R_{A0}}\right)^2 - \frac{2V_{\rm DD}}{\beta_{10} R_{A0}}}}\right] \\ N &= V_{\rm IN} - V_{\rm TH10} + \frac{1}{\beta_{10} R_{A0}} - \sqrt{(V_{\rm IN} - V_{\rm TH10} + \frac{1}{\beta_{10} R_{A0}})^2 - \frac{2V_{\rm DD}}{\beta_{10} R_{A0}}} \end{aligned} \tag{8}$$

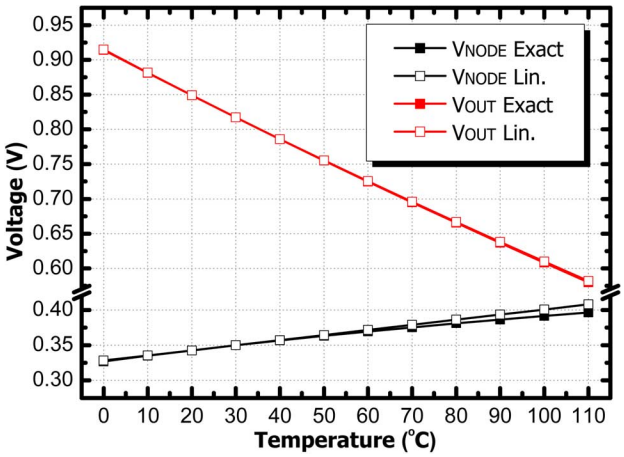

Fig. 5. Exact and linearized expressions for $V_{\rm NODE}$ and $V_{\rm OUT}$ against temperature.

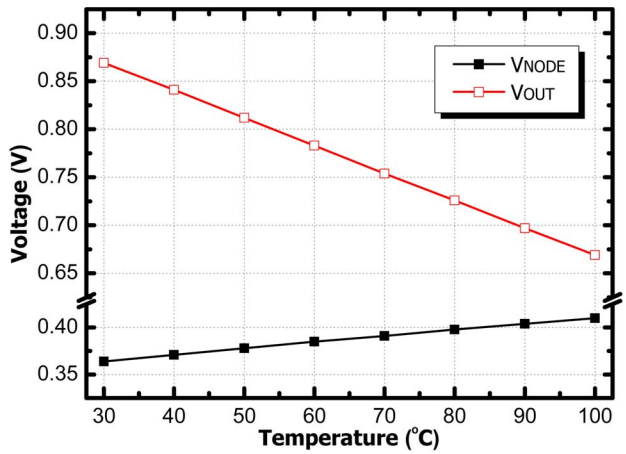

Fig. 6. Simulated $V_{\rm NODE}$ and $V_{\rm OUT}$ of the temperature sensor.

We see that $V_{\rm OUT}$ decreases linearly as the temperature increases. The slope $M + P$ of $V_{\rm OUT}$ against temperature is mainly dependent on the value of $\alpha_{\rm VTH1}$, $\alpha_{\rm VTH2}$ and the ratio of $R_{\rm D0}$ to $R_{\rm S0}$. Since these values are fairly tolerant to process variation, the slope of $V_{\rm OUT}$ should remain close to its intended value. The offset of $V_{\rm OUT}$ is determined by $V_{\rm IN}$, which can easily be adjusted after fabrication. These relationships enable us to use one-point calibration, which greatly reduces the time and the complexity of the mass production line.

To demonstrate that the accuracy of the linearized (13) is directly applicable to our temperature sensor circuit design, we present output voltages derived from (3), (8), (11) and (12) in Fig. 5. The m is set to 2, $\alpha_{\rm VTH1}$ and $\alpha_{\rm VTH2}$ are 0.00144 mV/°C, and $\alpha_{\rm R}$ is 0.157%/°C. The threshold voltages $V_{\rm TH10}$ and $V_{\rm TH20}$ are 0.16 and 0.156 V respectively. The characteristics of M_1 and M_2 are determined by β_{10} and β_{20}, which are set to 0.108 and 5.9 mA/V^2, respectively. The supply voltage $V_{\rm DD}$ is 1.1 V, and the input voltage $V_{\rm IN}$ supplied to M_1 is 0.85 V. T_0 is assumed to be 25 °C. The values of the resistors $R_{\rm A0}$, $R_{\rm D0}$, and $R_{\rm S0}$ are, respectively, 39, 100, and 60 kΩ. The calculated drain currents of M_1 and M_2 are 19.3 and 2.7 μA, respectively.

As shown in Fig. 5, the results of the linear approximation of (8) and (12) accord well with those of the exact (3) and (11). Since our initial design, based on those equations, relies on a square-law model of the transistor, it cannot be directly implemented in a modern deep submicron process. However, using the intuition provided by the linearized expressions, we can reach a final design quickly by trimming the values of $R_{\rm D0}$ and $R_{\rm S0}$ to adjust the slope and the values of $R_{\rm S0}$ and $V_{\rm IN}$ to adjust the offset of the voltage-temperature curve. Results obtained from a Spice simulation of the finalized design are shown in Fig. 6.

TABLE I
DESIGN SUMMARY OF THE TEMPERATURE SENSOR

Process	44nm DRAM
Supply voltage ($V_{\rm DDSENSOR}$)	1.1V
Operating range	0°C – 110°C
Temperature sensitivity	−3.2mV/°C
Resolution (with a 6.2mV resistor ladder step)	1.94°C
Calibration (35°C – 105°C)	One-point
Accuracy (From 61 samples after calibration)	−1.42°C ~ +2.66°C
Area	0.001725mm^2 (115μm x 15μm)
Average power dissipation	0.36μW (0.33μA x 1.1V)

$$V_{\rm OUT}(T) \simeq V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[V_{\rm NODE} + P(T - T_0) + Q\right]$$
$$P = \alpha_{\rm VTH2} + \frac{1}{\beta_{20} R_{S0} T_0}\left[(m - \alpha_R T_0)\left\{1 - \sqrt{1 + 2\beta_{20} R_{S0}(V_{\rm NODE} - V_{\rm TH20})}\right\} + \frac{\beta_{20} R_{S0}\{\alpha_{VTH2} T_0 + (m - \alpha_R T_0)(V_{\rm NODE} - V_{\rm TH20})\}}{\sqrt{1 + 2\beta_{20} R_{S0}(V_{\rm NODE} - V_{\rm TH20})}}\right]$$
$$Q = -V_{\rm TH20} + \frac{1}{\beta_{20} R_{S0}}\left[1 - \sqrt{1 + 2\beta_{20} R_{S0}(V_{\rm NODE} - V_{\rm TH20})}\right] \quad (12)$$

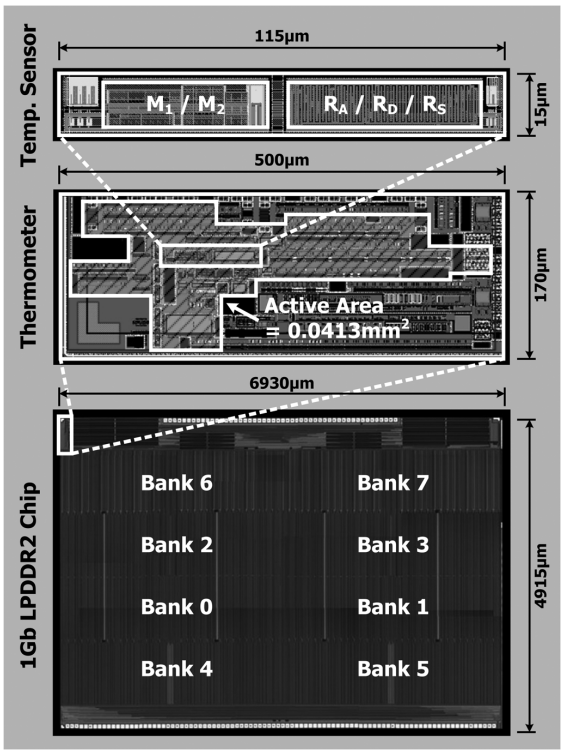

Fig. 7. Microphotograph of the 1-Gb LPDDR2 chip and magnified layouts of the thermometer and sensor.

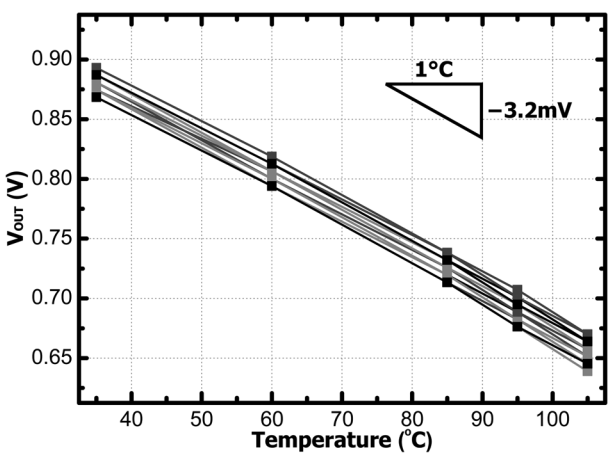

Fig. 8. Measured output voltages from 61 samples of the sensor circuit before one-point calibration, with their average slope.

IV. Experimental Results

A prototype thermometer was designed and fabricated on a 1-Gb LPDDR2 in a 44-nm DRAM process, with the characteristics summarized in Table I. Fig. 7 shows a microphotograph of the fabricated chip, with its thermometer located at the upper left corner. The area of the thermometer is approximately 0.0413 mm^2, and the temperature sensor occupies 0.001725 mm^2 of that. The drain currents through M_1 and M_2 in the sensor are 19 and 1.8 μA, respectively; but, since the sensor is only activated for 128 μs in every 8-ms cycle, it consumes 0.33 μA on average.

Fig. 8 shows the variation of output voltages against temperature, for 61 samples of the sensor circuit. Between 35 °C and 105 °C, the sensors exhibit a temperature sensitivity of

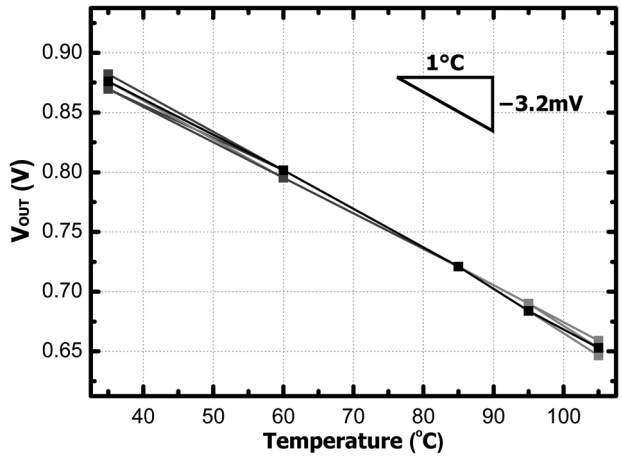

Fig. 9. Measured output voltages from 61 samples of the sensor circuit after one-point calibration, with their average slope.

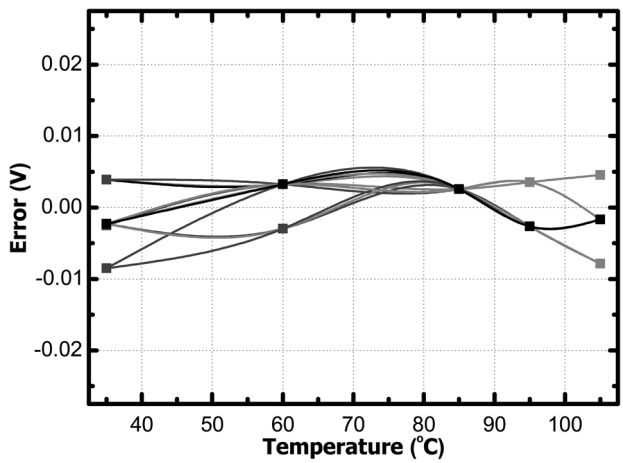

Fig. 10. Measured voltage error after the one-point calibration.

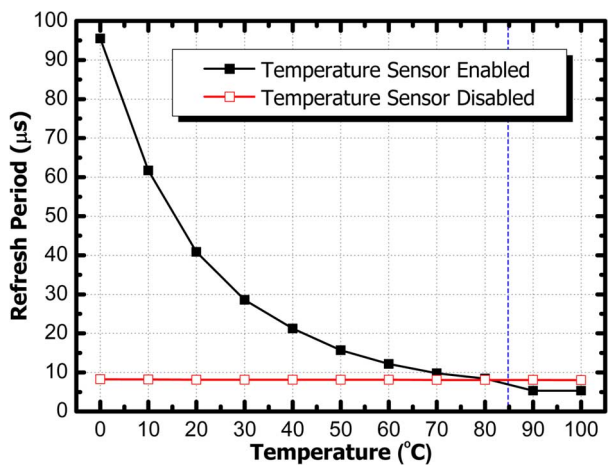

Fig. 11. Measured refresh period against temperature, with and without refresh period control.

−3.2 mV/°C on average, which is not affected by process variation. With this gain, the 6.2-mV step of the resistor ladder provides a resolution of 1.94 °C. The uniformity of the temperature sensitivity, provided by the theoretical analysis, permits one-point calibration. Since the refresh rate needs to be precisely controlled at higher temperatures, the target temperature for the calibration is chosen to set to 85 °C. Fig. 9 shows the

TABLE II
COMPARISON WITH PREVIOUSLY PUBLISHED WORKS

	This work	Kim, CICC, 2009 [16]	Kim, ISCAS, 2008 [17]	Souri, ESSCIRC, 2011 [18]	Shalmany, ISSCC, 2013 [19]
Calibration	One-point	One-point	One-point	Two-point	One-point
Process	44mn DRAM	65nm CMOS	80nm DRAM	0.16μm CMOS	0.13μm CMOS
Supply voltage (V)	1.1	1.2	N/A	1.8	1.5
Temperature range (°C)	0 ~ +110	−40 ~ +110	0 ~ +100	−55 ~ +125	−55 ~ +85
Accuracy (°C) (# of samples)	−1.42 ~ +2.66 (61)	−2.899 ~ +2.748 (15)	N/A	± 0.1 (20)	±0.15 (12)
Resolution (°C)	1.94	0.34	0.7	0.033	0.005
Conversion rate (S/s)	125	366k	1	5	50
Power consumption (μW)	0.36	400	< 1	8.6	55
Area (mm^2)	0.0413 (0.001725)	0.0066 (0.0013)	0.016	0.12	1.1

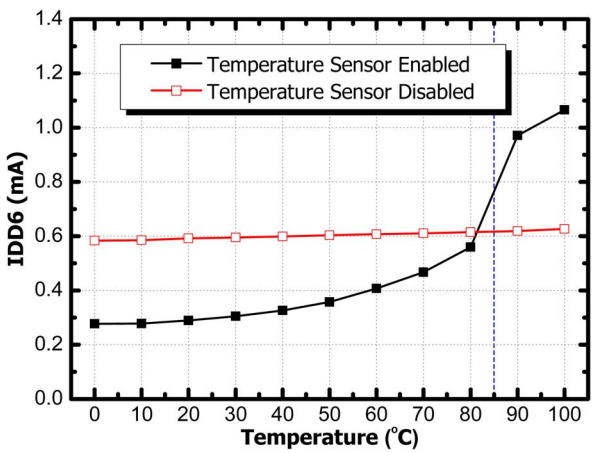

Fig. 12. Measured IDD6 current against temperature, with and without refresh period control.

output voltages of the 61 samples after the one-point calibration. The temperature sensitivity is unchanged since one-point calibration simply adjusts the dc level of each output. Fig. 10 shows the voltage error after calibration, which ranges between −8.5 and +4.53 mV, corresponding to a temperature error between −1.42 °C and +2.66 °C.

Fig. 11 shows how our thermometer changes the self-refresh period of the LPDDR2 chip. The self-refresh period is designed to be 8 μs around 85 °C. With the sensor disabled, it stays 8 μs at this length; but with the sensor enabled, the period extends to 95 μs as the temperature drops to 0 °C. A longer refresh period reduces the temperature-dependent self-refresh current IDD6, as shown in Fig. 12. IDD6 stays at approximately 0.6 mA when there is no refresh control, but when self-refresh control is applied it drops to 0.33 mA at 40 °C and 0.28 mA at 0 °C. The self-refresh period should be shortened at high temperatures so that DRAM cells retain their data. With the sensor disabled, the period stays at 8 μs, which has the risk of data loss at higher temperature. With the sensor enabled, the period is shortened to 4 μs, which prevents data loss at the cost of increased IDD6.

Table II compares our temperature sensor with previously published works [16]–[19]. Our requirements of accuracy and resolution are relaxed, while the importance of one-point calibration, DRAM process, low power consumption, and small area implementation is emphasized.

V. CONCLUSION

We have presented an on-chip CMOS thermometer, incorporating a novel temperature sensor, for adjusting the self-refresh period of LPDDR2 memory. The sensor in the thermometer has a high temperature sensitivity and low sensitivity to the process variation because it only uses NMOS transistors and n+ active resistors.

We derived a linearized expression for the sensor output voltage which showed that the temperature sensitivity is robust to process variation and the offset is easily tunable after manufacturing. This permits one-point calibration, which can significantly improve productivity in mass production.

We incorporated our sensor into an LPDDR2 chip fabricated in a 44-nm DRAM process. We demonstrated that this thermometer adjusts the self-refresh period correctly as the temperature changes; and the IDD6 current is almost halved at the lowest operating temperature.

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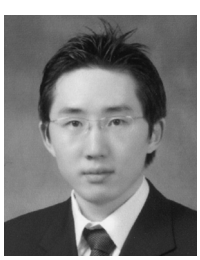
Daeyong Shim received the B.S. degree in electronic materials engineering from Korea Advanced Institute of Science and Technology, Seoul, Korea, in 1993, and the M.S. degree in inorganic materials engineering and Ph.D. degree in electrical engineering from Seoul National University, Seoul, in 1995 and 2013, respectively.

He joined Hyundai Electronics Co. Ltd. (now SK Hynix Semiconductor), Ichon, Korea, where he was involved in device and application engineering for DRAM. In 2008, he was charge of mobile product engineering team for the development of mobile DRAM products. Now, he is in charge of mobile product engineering group and focuses on low-power mobile DRAM design and test methodology.



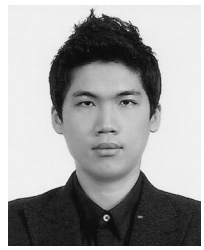
Hyunsik Jeong received the B.S. and M.S. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 2006 and 2008, respectively.

In 2008, he joined SK Hynix, Ichon, Korea, where he was engaged in DRAM design. Since 2013, he has been involved with the design of NAND Flash. His research interests are in temperature compensation circuits and low-power and high-speed memories.

Hyunjoong Lee (S'06–M'13) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2005, 2007, and 2012, respectively.

He is currently a Post-Doctoral Researcher with Seoul National University, Seoul, Korea. His current research interests include sensor interface for MEMS and bio-applications, data converter and analog techniques in CMOS circuits.

Dr. Lee was a recipient of the Gold Paper Award of the IEEE Seoul Section Student Paper Contest in 2009 and the Best Paper Award of the International Symposium on Low Power Electronics and Design in 2011.



Cyuyeol Rhee received the B.S. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2011. He is currently working toward the Ph.D. degree at Seoul National University, Seoul, Korea.

His research interests are in analog and mixed-signal integrated circuits and systems.

Deog-Kyoon Jeong (SM'09) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1981 and 1984, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1989.

From 1989 to 1991, he was with Texas Instruments, Dallas, TX, USA, as a Member of the Technical Staff, where he worked on single-chip implementation of the SPARC architecture. He joined the faculty of the Department of Electronics Engineering and Inter-University Semiconductor Research Center, Seoul National University, Seoul, Korea, where he is currently a Professor. He is one of the co-founders of Silicon Image, which specializes in digital interface circuits for video displays such as DVI and HDMI. His main research interests include the design of high-speed I/O circuits, phase-locked loops, and power conversion circuits.

Dr. Jeong was one of recipients of ISSCC Takuo Sugano Award in 2005 for Outstanding Far-East Paper.

Suhwan Kim (SM'08) received the B.S. and M.S. degrees in electrical engineering and computer science from Korea University, Seoul, Korea, in 1990 and 1992, respectively, and the Ph.D. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, MI, USA, in 2001.

From 1993 to 1999, he was with LG Electronics, Seoul, Korea. From 2001 to 2004, he was a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. In 2004, he joined Seoul National University, Seoul, Korea, where he is currently a Professor of electrical engineering. His research interests encompass analog and mixed signal circuits and device/circuit co-design opportunities.

Prof. Kim was the recipient of the 1991 Best Student Paper Award of the IEEE Korea Section, the First Prize (Operational Category) in the VLSI Design Contest of the 38th ACM/IEEE Design Automation Conference, and the 2011 Best Paper Award of the International Symposium on Low-Power Electronics and Design. He served as a guest editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS Special Issue on IEEE Asian Solid-State Circuits Conference. He has also served as the general co-chair and technical program chair for the IEEE International SOC Conference. He has participated on the technical program committee of the IEEE International SOC Conference, the International Symposium on Low-Power Electronics and Design, the IEEE Asian Solid-State Circuits Conference, and the IEEE International Solid-State Circuits Conference.